

What is claimed is:

1. A semiconductor device comprising:

a base frame having a first surface, and a second surface which opposes said first surface, and having an opening portion
5 through formed the base frame;

a semiconductor chip which has a first main surface on which a plurality of electrode pads is provided and a second main surface opposing said first main surface, and which is disposed within said opening portion such that the level of
10 said first main surface is substantially equal to the level of said first surface;

an insulating film formed on said first surface and said first main surface such that a part of each of said plurality of electrode pads is exposed;

15 a plurality of wiring patterns which are electrically connected to said plurality of electrode pads, respectively and which extend from said electrode pads to the upper side of the first surface of said base frame, respectively;

a sealing portion formed on said wiring patterns and said
20 insulating film such that a part of each of said wiring patterns is exposed; and

a plurality of external terminals provided over said wiring patterns in a region including the upper side of said base frame.

25 2. The semiconductor device according to claim 1, wherein said external terminals are arranged in a region over the upper side of said first surface at a first pitch wider

than a second pitch at which said electrode pads are arranged.

3. The semiconductor device according to claim 1, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals, wherein said sealing portion is formed such that a top surface of said electrode posts is exposed.

4. The semiconductor device according to claim 3, wherein said electrode posts are made from a conductive material.

5. The semiconductor device according to claim 4, wherein a thin oxidation layer is formed on the top surface of said electrode posts.

6. The semiconductor device according to claim 1, further comprising a lower base for supporting the second main surface of said semiconductor chip and the second surface of said base frame.

7. The semiconductor device according to claim 1, wherein said base frame comprises inside walls which define said opening portion, the thickness of the inside walls gradually decreasing toward said semiconductor chip.

8. The semiconductor device according to claim 1, wherein a portions of said wiring patterns on a boundary and vicinity thereof between a region on the upper side of said semiconductor chip and the base flame are formed wider or more thickly than other portions of said wiring patterns.

9. The semiconductor device according to claim 1, wherein said base frame comprises a plurality of through holes

and an inter-layer wiring which is made from a conductive material and is formed in the holes.

10. A semiconductor device comprising:

a base frame having a first surface, and a second surface
5 which opposes said first surface, and having an opening portion through formed the base frame;

a first semiconductor chip which has a first main surface on which a plurality of first electrode pads are provided and a second main surface opposing said first main surface, and
10 which is disposed within said opening portion such that the level of said first main surface is substantially equal to the level of said first surface;

a first insulating film formed on said first surface and said first main surface such that a part of each of said first
15 electrode pads is exposed;

a plurality of first wiring patterns which are electrically connected to said plurality of first electrode pads, respectively and which extend from said first electrode pads to the upper side of the first surface of said base frame,
20 respectively;

a first sealing portion formed on said first wiring patterns and said first insulating film such that a part of each of said first wiring patterns is exposed;

a plurality of first external terminals provided over
25 said first wiring patterns in a region including said first surface of said base frame;

a second semiconductor chip which has a third main surface

on which a plurality of second electrode pads are provided and a fourth main surface opposing said third main surface, and which is disposed within said opening portion such that the level of said third main surface is substantially equal to the level of said second surface;

a second insulating film formed on said second surface and said third main surface such that a part of each of said plurality of second electrode pads is exposed;

a plurality of second wiring patterns which are electrically connected to said plurality of second electrode pads, respectively and which extend from said second electrode pads to the upper side of the second surface of said base frame, respectively;

a second sealing portion formed on said second wiring patterns and said second insulating film such that a part of each of said second wiring patterns is exposed; and

a plurality of second external terminals provided on said second wiring patterns in a region including said second surface of said base frame.

11. The semiconductor device according to claim 10, wherein said first and second external terminals are arranged in a region over said first and second surfaces at a first pitch wider than a second pitch at which said first and second electrode pads are arranged.

12. The semiconductor device according to claim 10, further comprising a plurality of first electrode posts provided between said first wiring patterns and said first

external terminals and a plurality of second electrode posts provided between said second wiring patterns and said second external terminals,

wherein said first sealing portion is formed such that
5 the top surface of said first electrode posts is exposed and said second sealing portion is formed such that the top surface of said second electrode posts is exposed.

13. The semiconductor device according to claim 10,
wherein said electrode posts are made from a conductive
10 material.

14. The semiconductor device according to claim 13,
wherein a thin oxidation layer is formed on a top surface of said electrode posts.

15. The semiconductor device according to claim 10,
15 wherein a portions of said wiring patterns on a boundary and vicinity thereof between said semiconductor chip and the base frame are formed wider or more thickly than other portions of said wiring patterns.

16. The semiconductor device according to claim 10,
20 wherein said base frame comprises inside walls which define said opening portion, the thickness of the inside walls gradually decreasing toward said semiconductor chip.

17. The semiconductor device according to claim 10,
wherein said base frame comprises:

25 a plurality of through holes which pass through said first surface to said second surface; and

an inter-layer wiring connection which is formed in said

through holes and connects said first wiring patterns to said second wiring patterns.